



critical path target "Michael Hutton"

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Timing-driven placement for hierarchical programmable logic devices

M Hutton, K Adibsamii, A Leaver - Proceedings of the 2001 ACM/SIGDA ninth international ..., 2001 - portal.acm.org

... **Michael Hutton**, Khosrow Adibsamii and Andrew Leaver Altera Corporation 101 ... local allows us to better **target** the true ... we need to discuss **critical path** and slack ...Cited by 11 - [Web Search](#) - [mountains.ece.umn.edu](#) - [eecg.toronto.edu](#) - [portal.acm.org](#)Interconnect enhancements for a high-speed PLD architecture

M Hutton, V Chan, P Kazarian, V Maruri, T Ngai, J ... - FPGA, 2002 - portal.acm.org

... **Michael Hutton**, Vinson Chan, Peter Kazarian, Victor Maruri, Tony ... delay incurred by a **critical path** is common ... The **target** density for our architecture family is ...Cited by 5 - [Web Search](#) - [eecg.toronto.edu](#) - [sigda.org](#) - [acm.org](#) - [all 7 versions](#) »Adaptive delay estimation for partitioning-driven PLD placement

M Hutton, K Adibsamii, A Leaver - IEEE Transactions on Very Large Scale Integration(VLSI) ..., 2003 - ieeexplore.ieee.org

... Given a **target** delay (constraint) on an A to B ... most stringent constraint minus the actual delay of the **path**. ... A **critical path** is one which has the minimum slack ...Cited by 2 - [Web Search](#) - [portal.acm.org](#) - [portal.acm.org](#) - [dx.doi.org](#) - [all 5 versions](#) »Interconnect prediction for programmable logic devices

MD Hutton - SLIP, 2001 - portal.acm.org

... wires inefficiently if it allows a more **critical** connection to have even a slightly faster **path**. ... a given design, I implemented it in the **target** device (for ...Cited by 4 - [Web Search](#) - [eecg.toronto.edu](#) - [portal.acm.org](#)MAX II: A Low-Cost, High-Performance LUT-Based CPLD

P Leventis, B Vest, M Hutton, D Lewis, F ... - Custom Integrated Circuits Conference, 2004. Proceedings of ..., 2004 - ieeexplore.ieee.org

... CPLD Paul Leventis\*, Brad Vest, **Michael Hutton**, David Lewis ... smaller designs fall outside the **target** range of ... faster LUT inputs on the **critical path**, yielding a ...Cited by 1 - [Web Search](#) - [ieeexplore.ieee.org](#)Characterization and parameterized generation of synthetic combinational benchmark circuits

MD Hutton, J Rose, JP Grossman, DG Corneil - IEEE Transactions on Computer-Aided Design of Integrated ..., 1998 - ieeexplore.ieee.org

... Hence, each node lies on a unique directed **path** from the ... Step A.2(a): We first consider the "**critical**" unit edges ... First, calculate **target** fanouts, **target** , ...Cited by 14 - [Web Search](#) - [ieeexplore.ieee.org](#) - [csa.com](#)The Quartus University Interface Program: Enabling Advanced FPGA Research

S Malhotra, TP Borer, DP Singh, SD Brown - Field-Programmable Technology, 2004. Proceedings. 2004 IEEE ..., 2004 - ieeexplore.ieee.org

... ing the final operating performance of the **target** circuit ... the logic region to be non-**critical** may have ... to explore include the use of **path**-based approaches ...[Web Search](#) - [ieeexplore.ieee.org](#)



critical path target delay statistic "Altera Corpo

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Combining Technology Mapping and Placement for Delay-Optimization in FPGA Designs

CSCYW Tsay - [ieeexplore.ieee.org](http://ieeexplore.ieee.org)

... After initial mapping and placement, the **critical** blocks are ... is labelled the length of the longest **path** from any ... Each vertex  $v \in C$  represents a **target** CLB, 1db2 ...

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Combining Technology Mapping and Placement Delay-Optimization in FPGA Designs

CSCYW Tsay - [portal.acm.org](http://portal.acm.org)

... After initial mapping and placement, the **critical** blocks are identified for re ... longest **path** from any primary inputs to itself. ... ping candidate for each **target** CLB ...

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Combining Technology Mapping and Placement for Delay-Minimization in FPGA Designs

ACH Wu - [ieeexplore.ieee.org](http://ieeexplore.ieee.org)

... gate is labeled the length of the longest **path** from any ... of a seed node (sn) to a **target** CLB (tclb ... no-connection(mc)) -  $E_x$  (total wiring **delay**/no\_connection(mc) ...

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EMPAR: An Interactive Synthesis Environment for Hardware Emulations

TG Lee, WJ Fang, CHW Allen - [Synthesis-sigda.org](http://Synthesis-sigda.org)

... the con- straints of the **target** EM architecture ... design-quality analyzer to perform **critical delay** analysis ... Subsequent- ly, each **critical path** can be highlighted ...

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Virtual wires: overcoming pin limitations in FPGA-based logic emulation

JW Babb, R Tessier, A Agarwal - 1993 - [lcs.mit.edu](http://lcs.mit.edu)

... 7.11 Reduction Of **Critical Path** with Hybrid Wiring : : : : 83 ... characterized by their interconnection topology network , **target** **FPGA** processor ...

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Image processing PCI-based shared memory architecture design

D Houzet, A Fatni, JL Basille - The 1997 Conference on Computer Architectures for Machine ..., 1997 - [doi.ieeeecomputersociety.org](http://doi.ieeeecomputersociety.org)

... This second-level ring adds a 2-cycle **delay** of latency ... to the data, according to the **target** architecture, or ... adds to the length of the **critical path** through a ...

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PC-based shared memory architecture and language

D Houzet, A Fatni - J SUPERCOMPUT, 1998 - [kluweronline.com](http://kluweronline.com)

... This second-level ring adds a 2-cycle **delay** of latency ... according to the structure of the **target** architecture. ... adds to the length of the **critical path** through a ...

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Hardware Performance Simulations of Round 2 Advanced Encryption Standard Algorithms

B Weeks, M Bean, T Rozyłowicz, C Ficke - AES Candidate Conference, 2000 - [mirrors.wiretapped.net](http://mirrors.wiretapped.net)

... 2.1.1 **Target** Applications ... is a function of two parameters: the worst-case **path delay** between any two ... may minimize area while another may minimize **delay** time. ...

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Sigma-Dc.. Ita Modulation

ISP MAGAZINE - [ieeexplore.ieee.org](http://ieeexplore.ieee.org)

... Other features such as block memory and **delay**-locked-loop technology arc also significant factors that ... This generic **FPGA** ar- chitecture is shown iii Fmg. ...

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A Stream-Based Configurable Computing Radio Testbed

S Swanchara, S Harper, P Athanas - at the IEEE Symposium on Field Programmable Custom Computing ..., 1998 - [doi.ieeecs.org](http://doi.ieeecs.org)

... scheduled based upon the capabilities of the **target** CCM platform ... A stream is a **path** through the system that is ... the system, and is the most complex and **critical**. ...

Cited by 8 - Web Search - [ieeexplore.ieee.org](http://ieeexplore.ieee.org) - [doi.ieeecomputersociety.org](http://doi.ieeecomputersociety.org) - [ee.vt.edu](http://ee.vt.edu) - [all 9 versions »](#)

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IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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- ☐ 1. **Characterization and parameterized generation of synthetic combination circuits**  
Hutton, M.D.; Rose, J.; Grossman, J.P.; Corneil, D.G.;  
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction: Volume 17, Issue 10, Oct. 1998 Page(s):985 - 996  
Digital Object Identifier 10.1109/43.728919  
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(340 KB\)](#) IEEE JNL
- ☐ 2. **Automatic generation of synthetic sequential benchmark circuits**  
Hutton, M.D.; Rose, J.S.; Corneil, D.G.;  
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction: Volume 21, Issue 8, Aug. 2002 Page(s):928 - 940  
Digital Object Identifier 10.1109/TCAD.2002.800456  
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(398 KB\)](#) IEEE JNL
- ☐ 3. **Applications of clone circuits to issues in physical-design**  
Hutton, M.D.; Rose, J.;  
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Conference on  
Volume 6, 30 May-2 June 1999 Page(s):448 - 451 vol.6  
Digital Object Identifier 10.1109/ISCAS.1999.780191  
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- ☐ 4. **Equivalence classes of clone circuits for physical-design benchmarking**  
Hutton, M.D.; Rose, J.;  
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Conference on  
Volume 6, 30 May-2 June 1999 Page(s):428 - 431 vol.6  
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